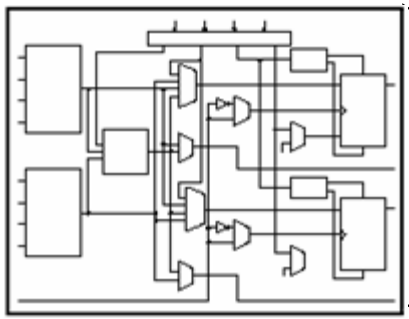

NATIONAL
INSTRUMENTS™

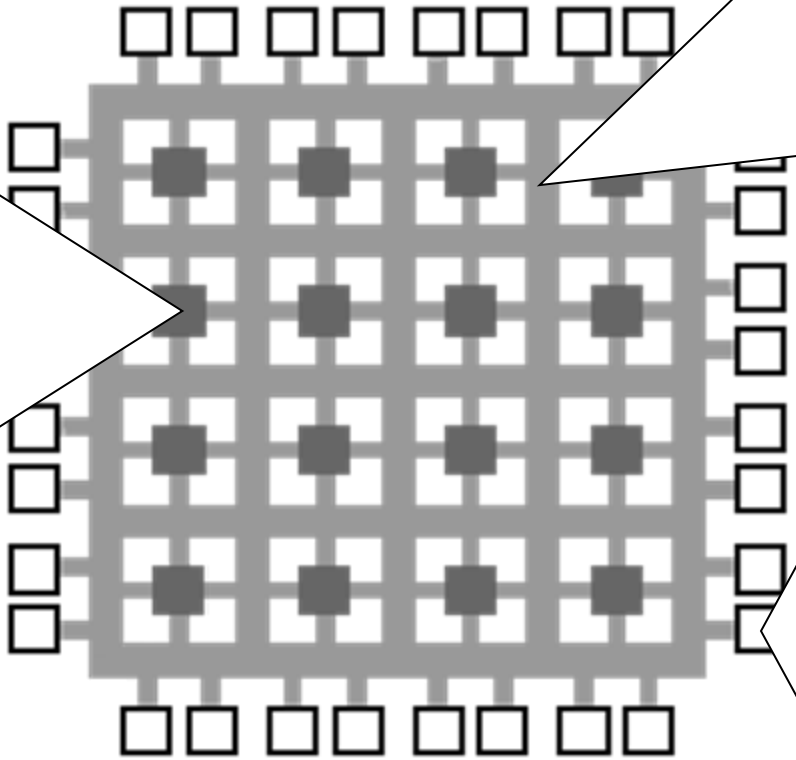
Agenda

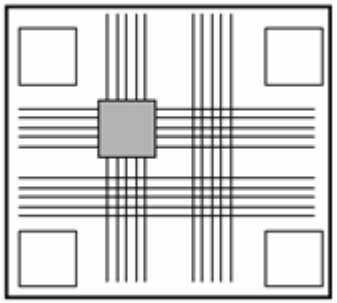
- **Programming FPGAs**
- Why Are They Useful?
- NI FPGA Hardware
- Common Applications for FPGAs
- How to Learn More

FPGA Technology

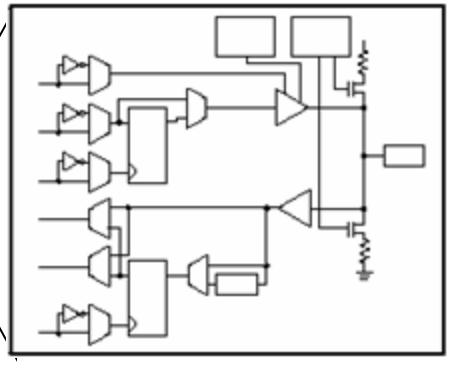


Logic Blocks





Programmable Interconnects

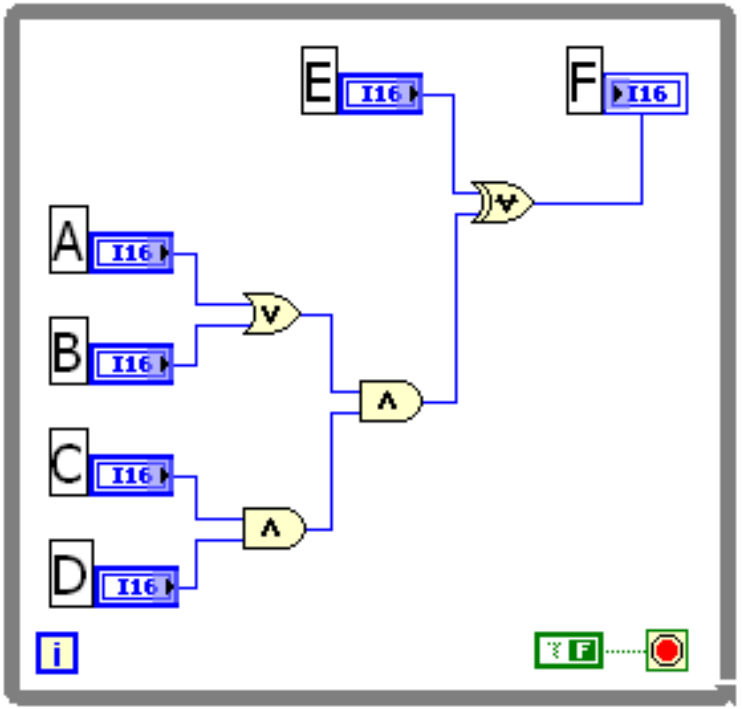


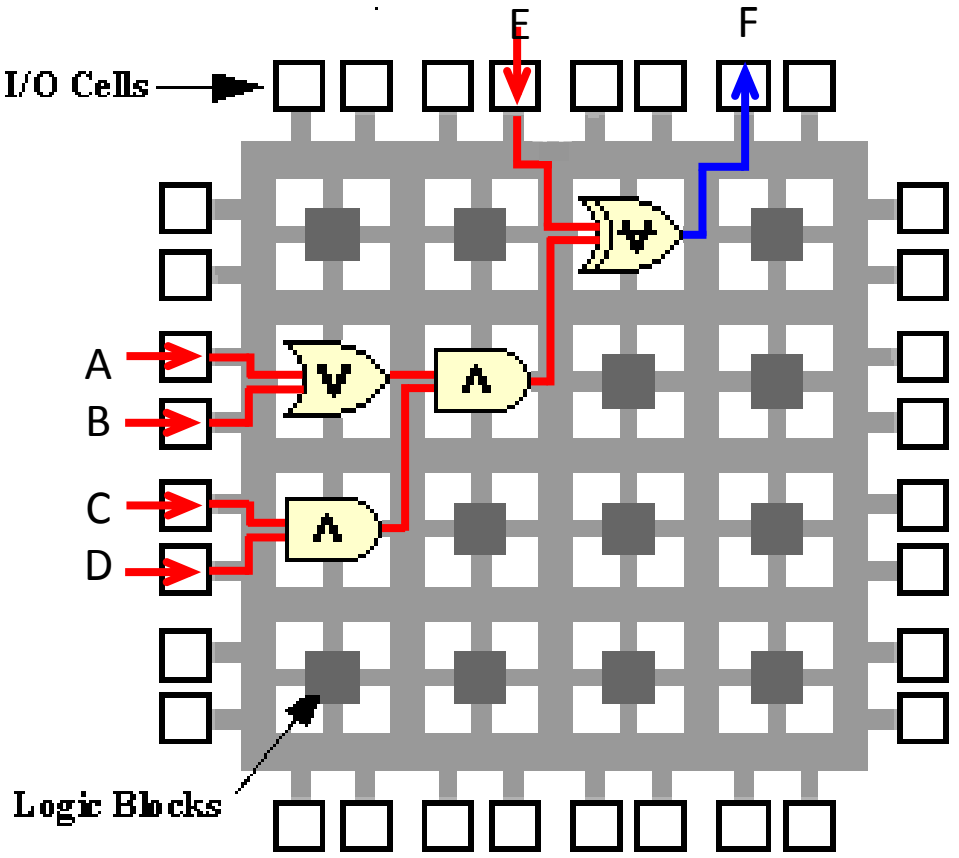
I/O Blocks

FPGA Logic Implementation

Implementing Logic on FPGA: F = {(A+B)CD} ⊕ E

LabVIEW FPGA Code





Demo

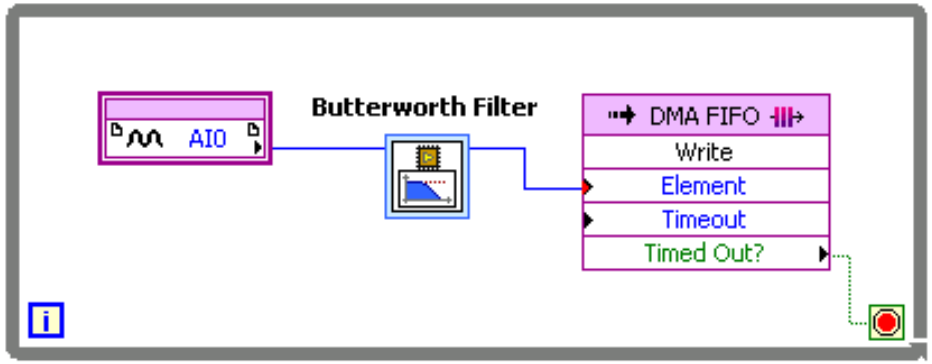
- Filter

LabVIEW FPGA Code Abstraction

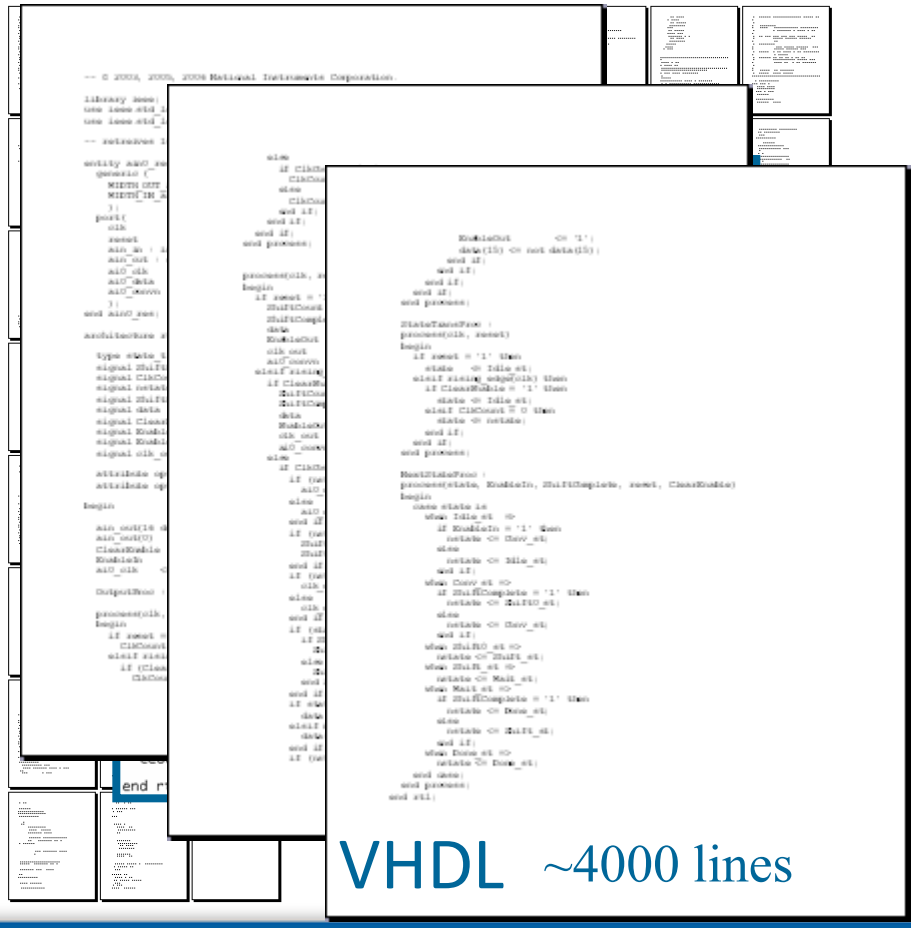
Counter

Analog I/O

I/O with DMA

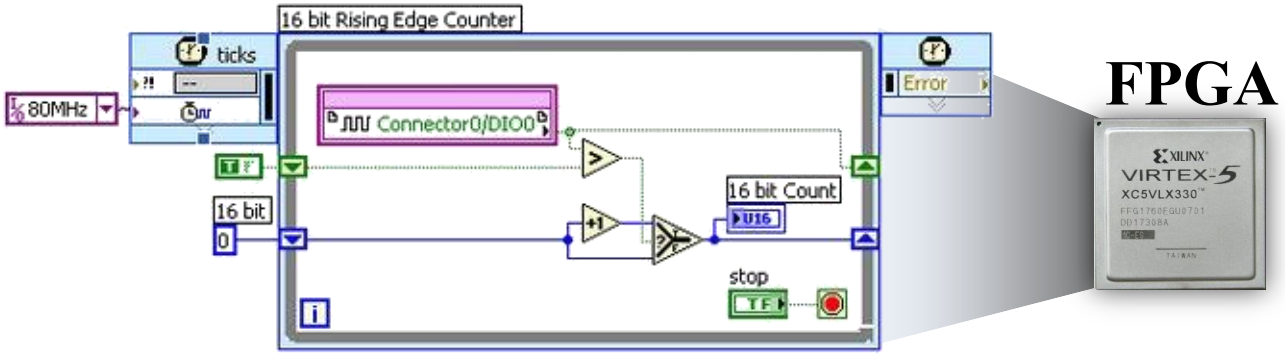


LabVIEW FPGA



VHDL ~4000 lines

LabVIEW FPGA Module



- LabVIEW code is translated to hardware circuitry implemented on the FPGA
- Natural representation of FPGA logic

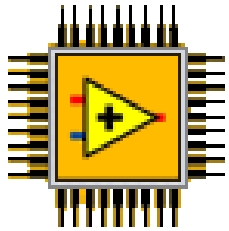
Demo

- Simple I/O

Agenda

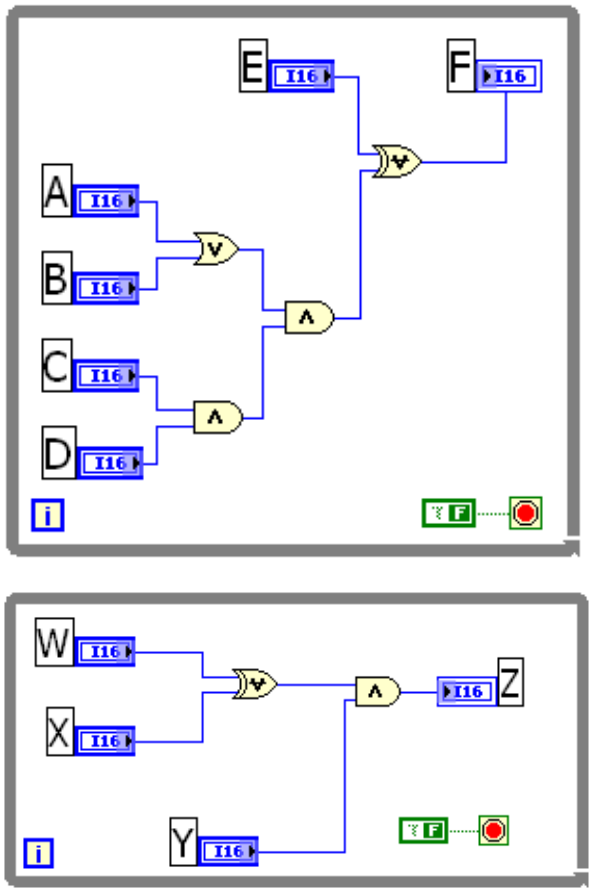
- Programming FPGAs
- **Why Are They Useful?**
- NI FPGA Hardware
- Common Applications for FPGAs
- How to Learn More

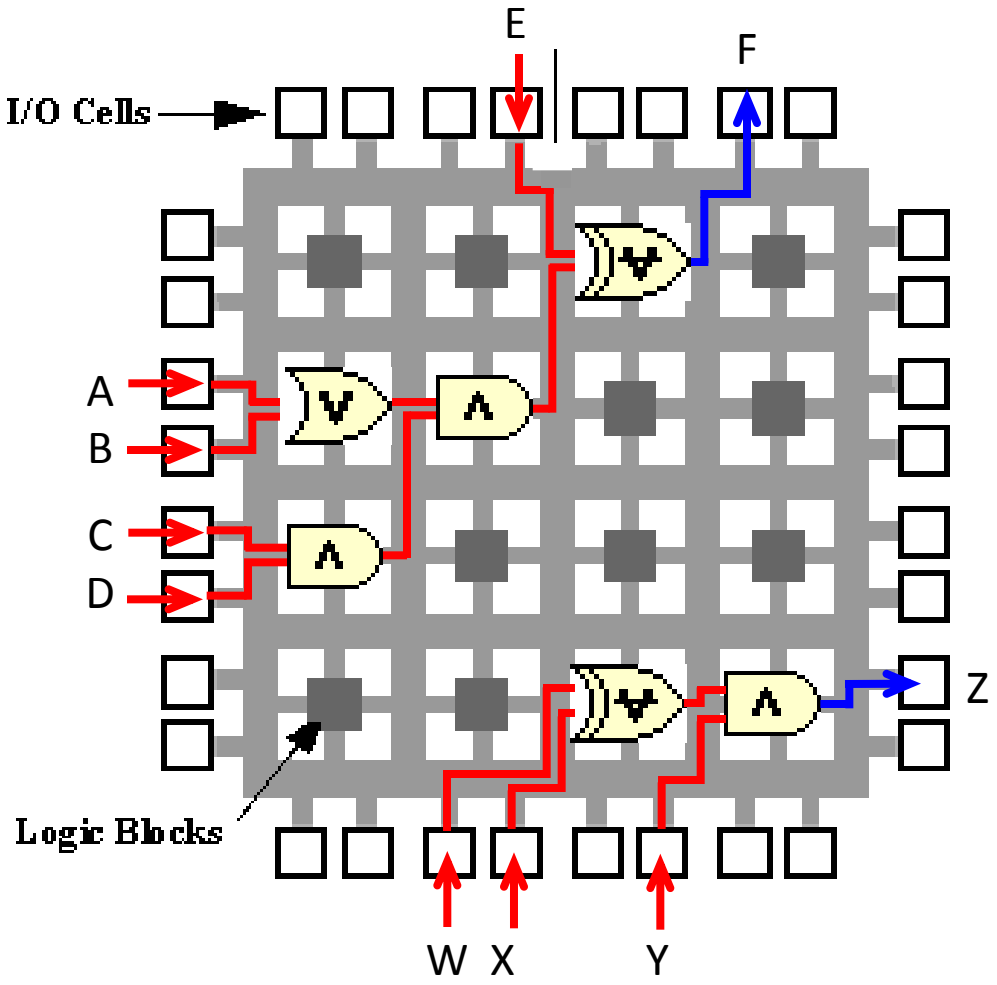
Why Are They Useful?



- ***True Parallelism*** – Provides parallel tasks and pipelining
- ***High Reliability*** – Designs become a custom circuit
- ***High Determinism*** – Runs algorithms at deterministic rates down to 25 ns (faster in many cases)
- ***Reconfigurable*** – Create new and alter existing task-specific personalities

True Parallelism

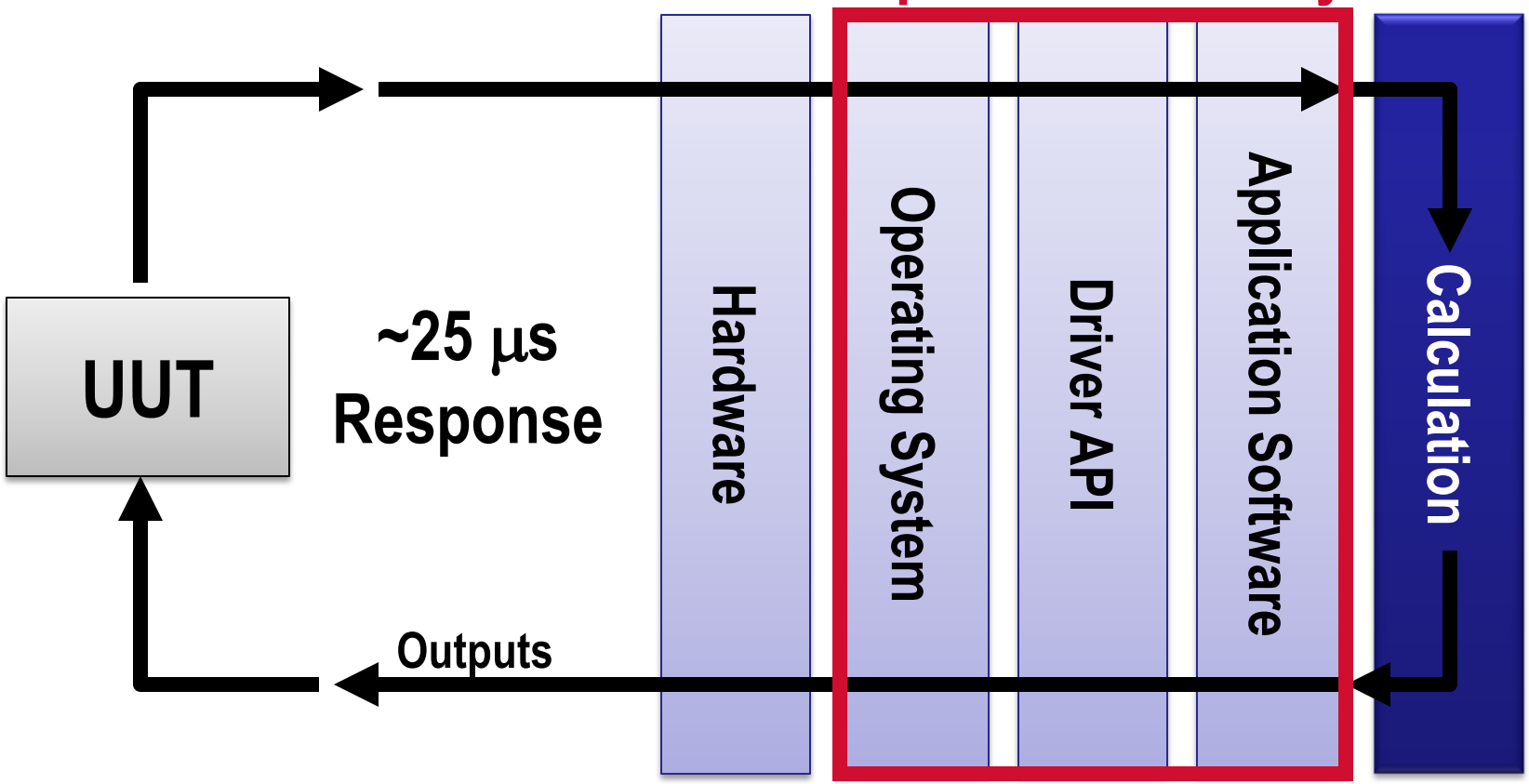




High Reliability and Determinism

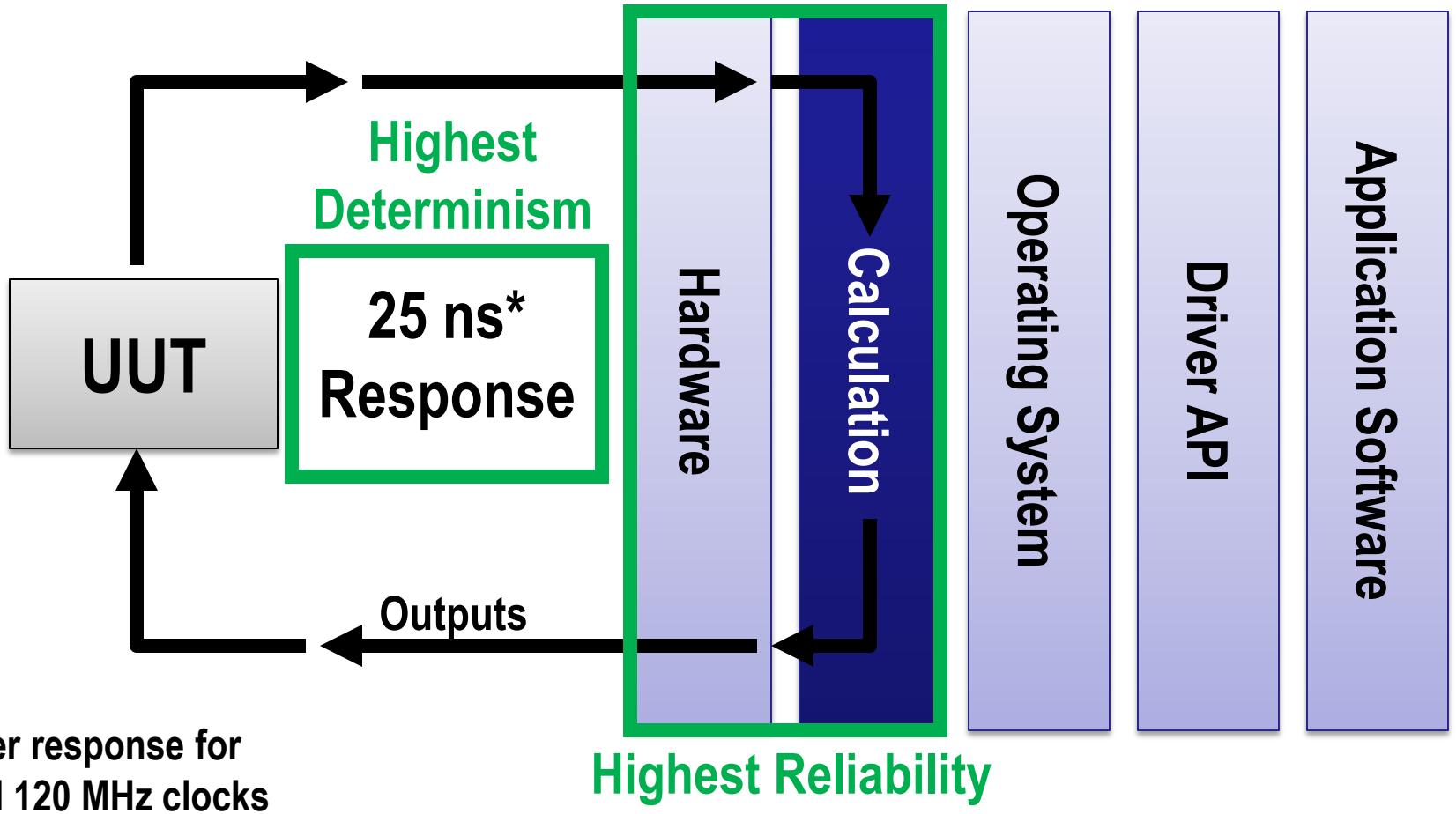
Decision Making in Software

Multiple Software Layers



High Reliability and Determinism

Decision Making in Hardware

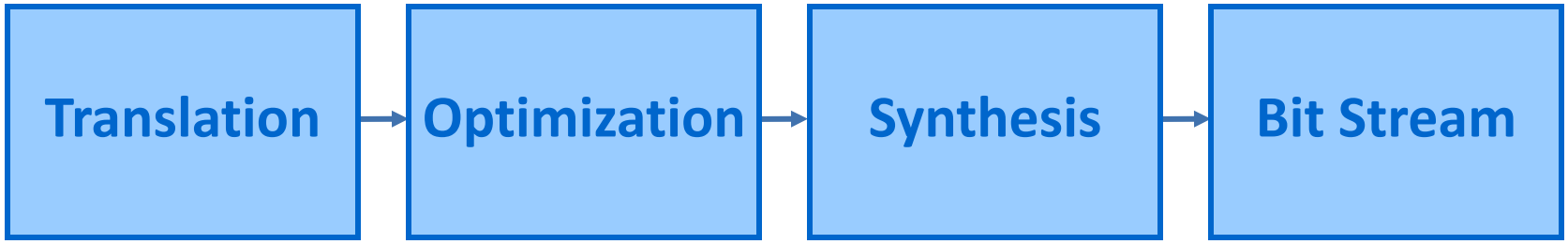


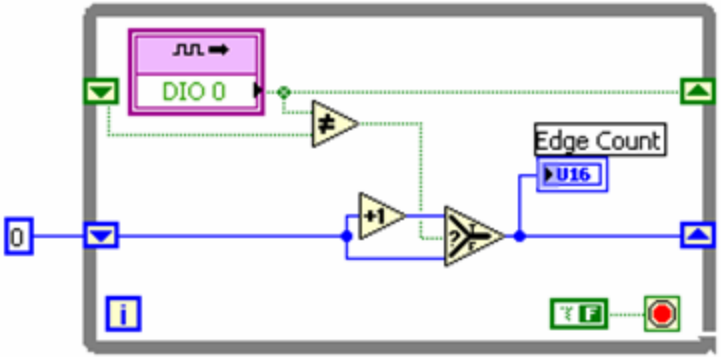
* Faster response for
80 and 120 MHz clocks

Demo

- AI, AO, Custom Threshold logic

From LabVIEW to Hardware





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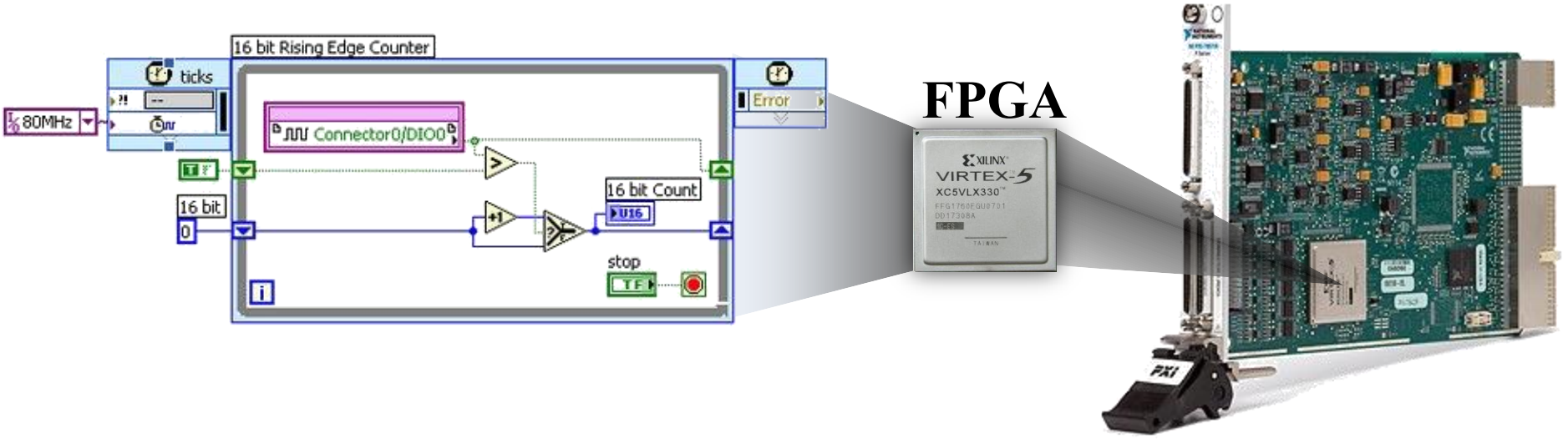
What Is RIO Technology?



- Use NI LabVIEW to design custom hardware circuitry with off-the-shelf devices

NI LabVIEW FPGA Hardware Targets

R Series Multifunction RIO

- General Purpose I/O for Measurement and Control

NI CompactRIO

- Industrial Control and Monitoring

NI SingleboardRIO

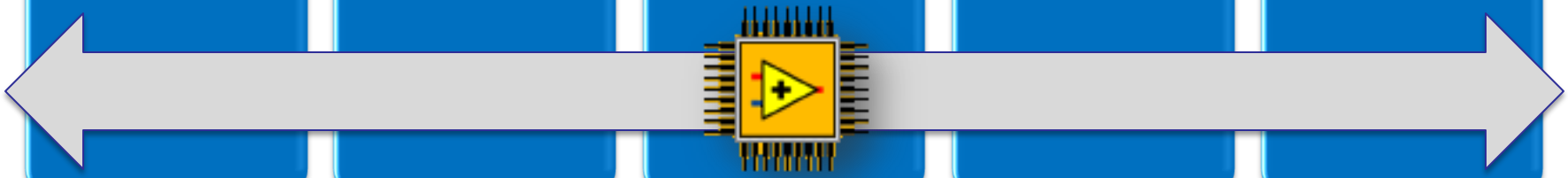
- Embedded Systems

NI FlexRIO

- Manufacturing Test and Design Validation

Other

- RIO IF Transceiver
- PCIe Framegrabbers
- Compact Vision System



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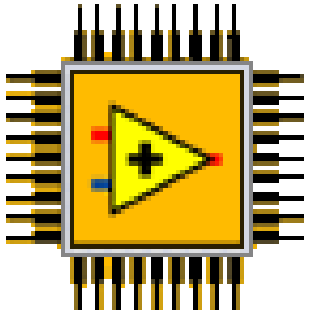
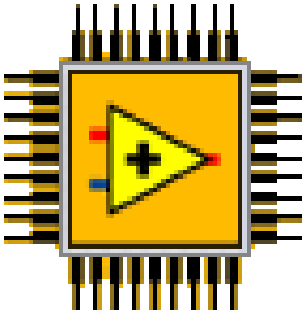
Common Applications



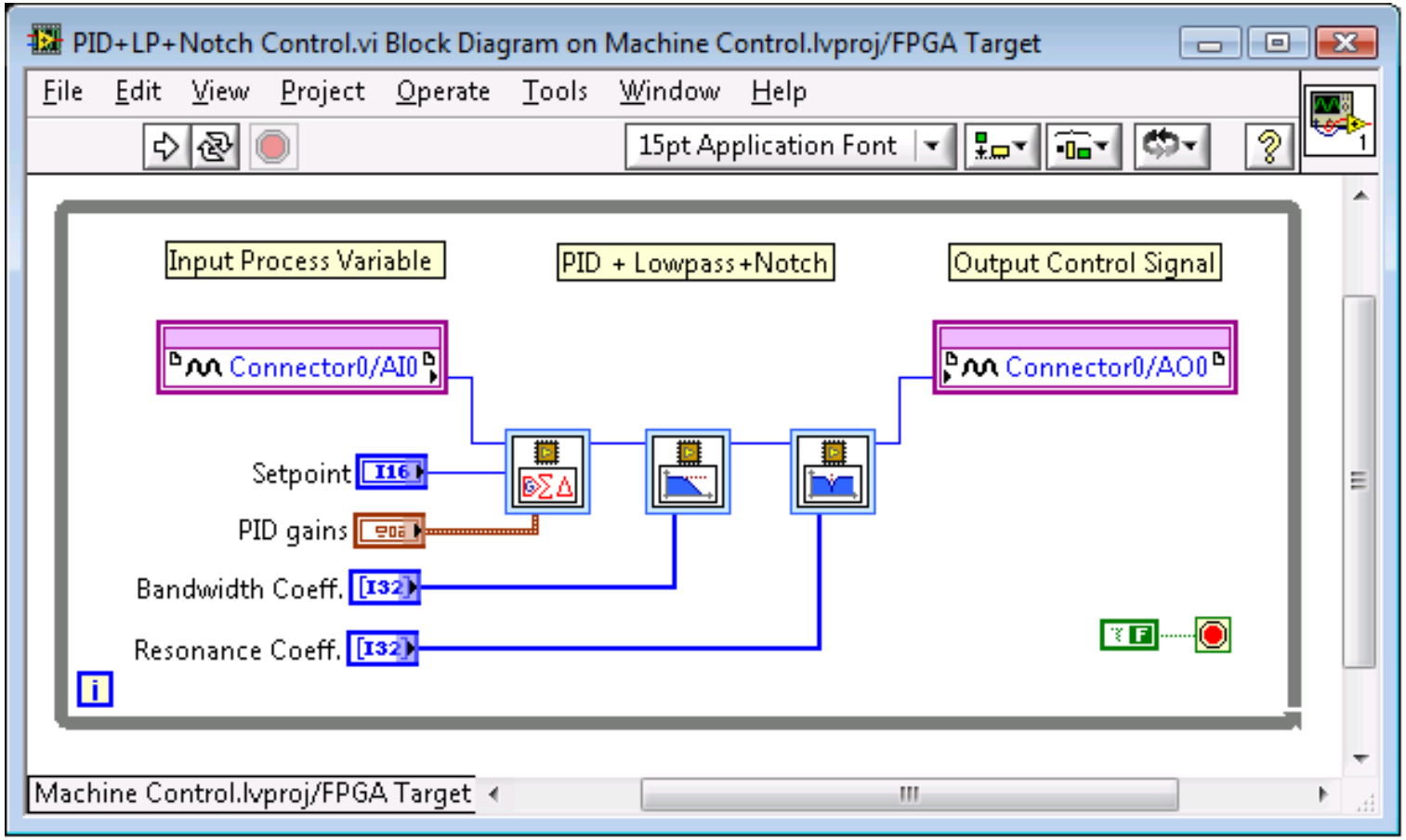
- High-speed control
- Custom DAQ
- Digital communication protocols
- Sensor simulation
- Onboard processing and data reduction

Common Applications



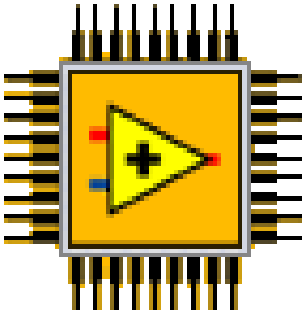
- High-speed control
- Custom DAQ
- Digital communication protocols
- Sensor simulation
- Onboard processing and data reduction
- Coprocessing

High-Speed Control



About 200 kHz loop rate

Common Applications



- High-speed control
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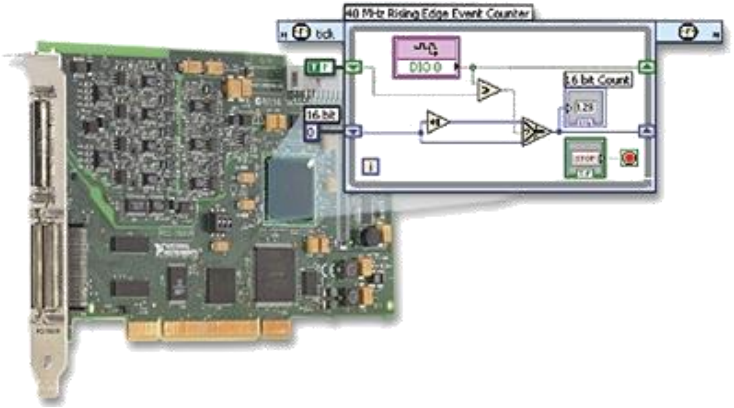
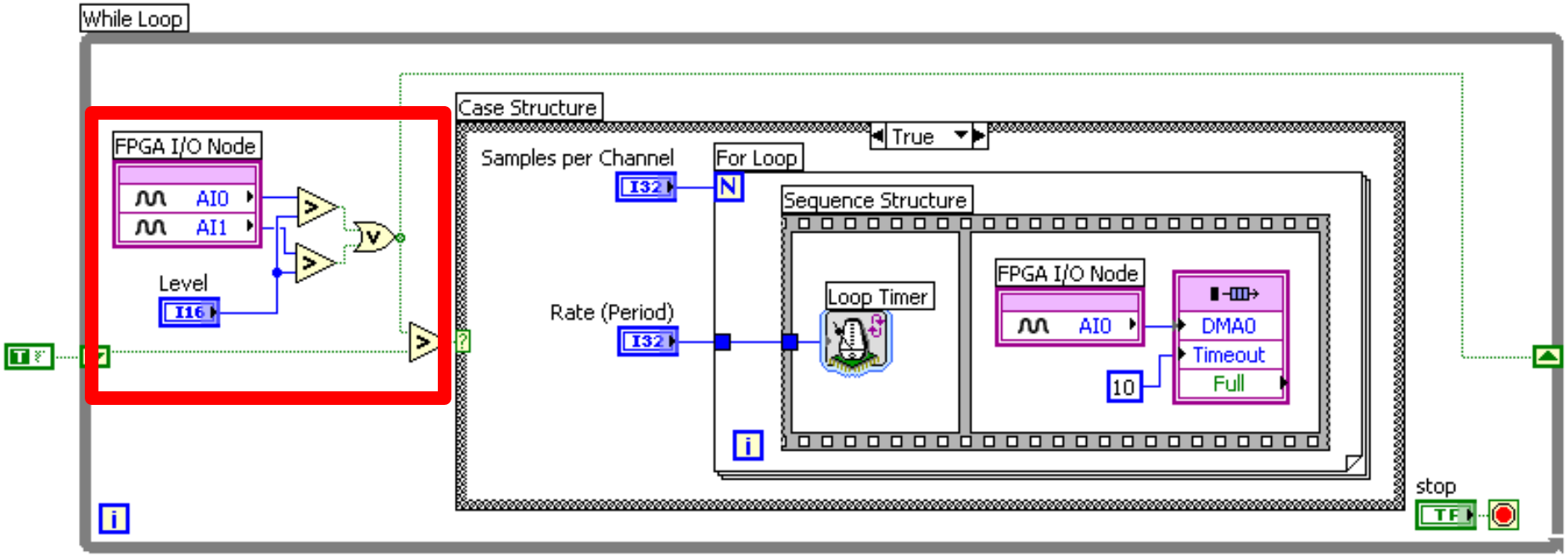
Customize Your DAQ Device

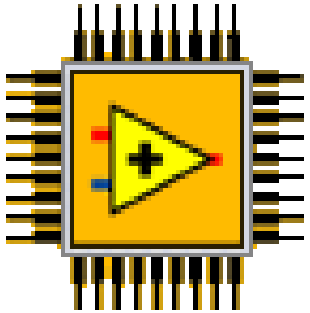
- Custom timing & synchronization
- Multi-rate sampling
- Custom triggering
- Custom counters
- Flexible PWM
- Flexible encoder interface



Custom Triggered Analog Input



Common Applications



- High-speed control
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- **Digital communication protocols**
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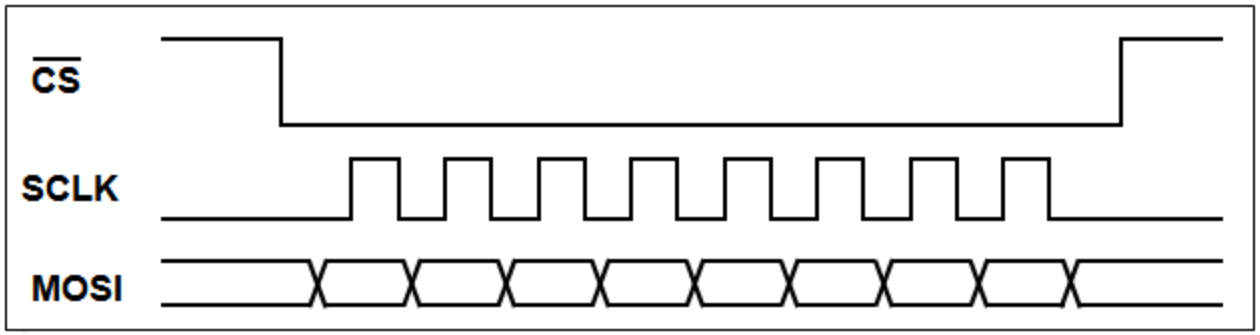
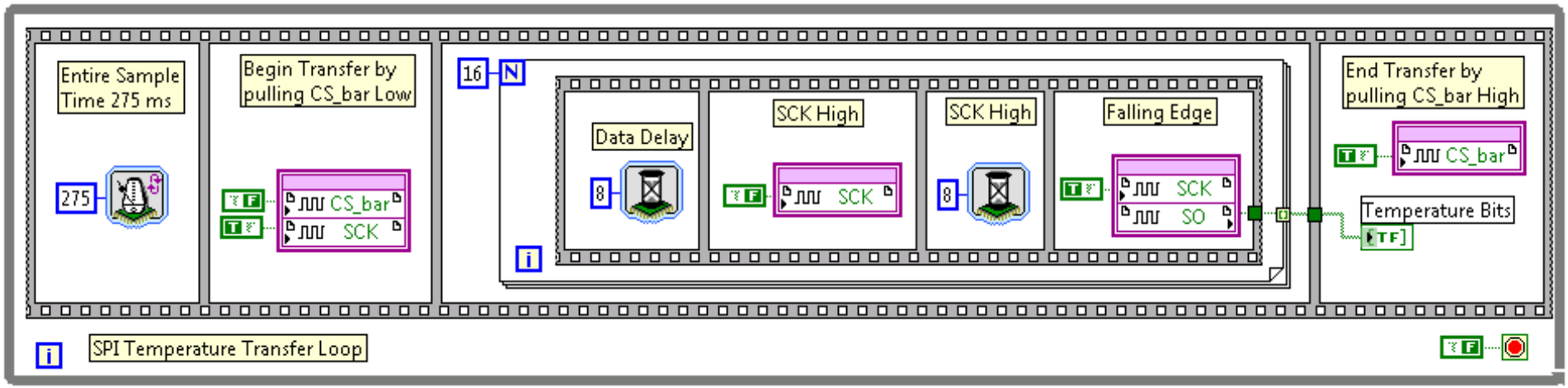
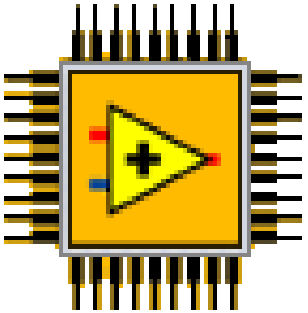
Digital Communication

Example – SPI





Common Applications



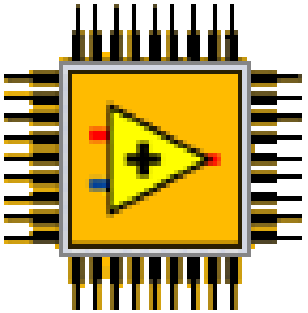
- High-speed control
- Custom DAQ
- Digital communication protocols
- **Sensor simulation**
- Onboard processing and data reduction

Sensor Simulation and FPGA

- Fully customizable hardware – Many types of sensors
- Parallelism – Many sensors on chip with no interference
- Strict timing requirements – Deterministic or highly realistic
- Onboard processing – Engineering units to sensor signals

Sensor Signals

Common Applications



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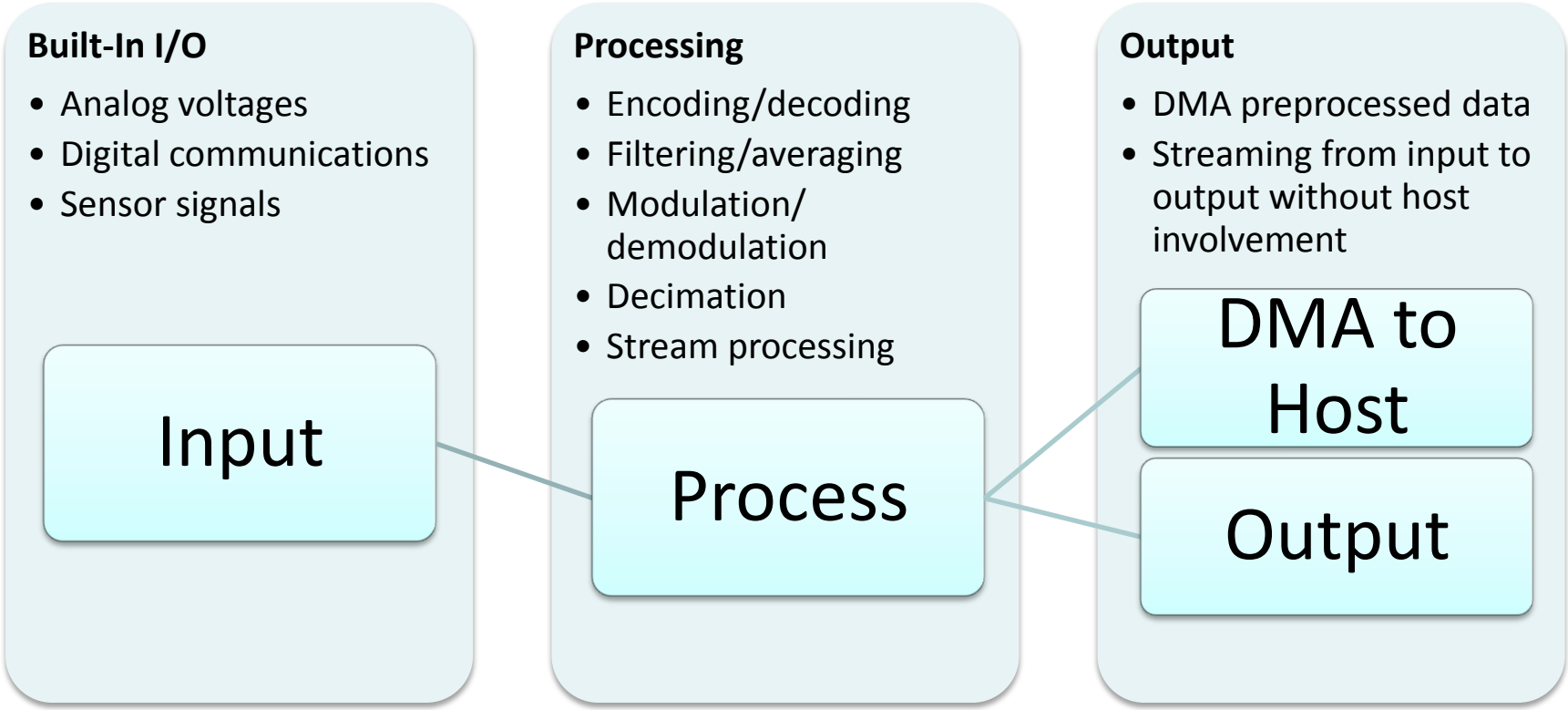
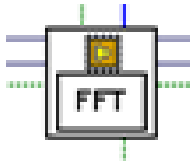
Onboard Processing and Data Reduction

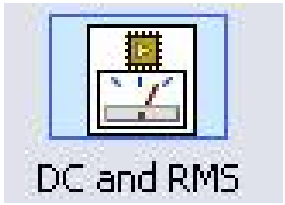


Intellectual Property (IP)

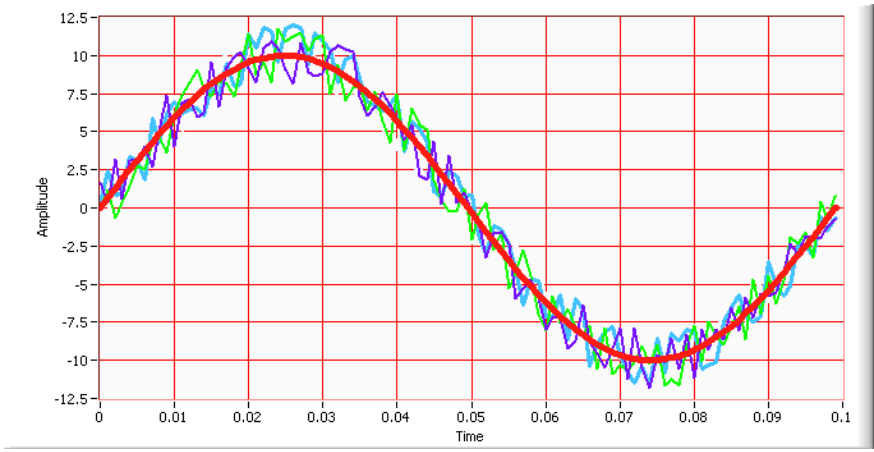
FFT



DC/RMS

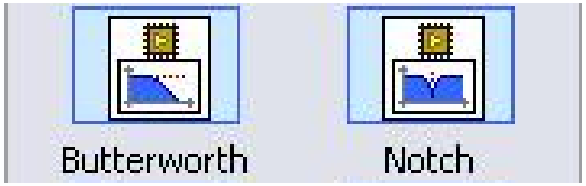


Waveform Averaging

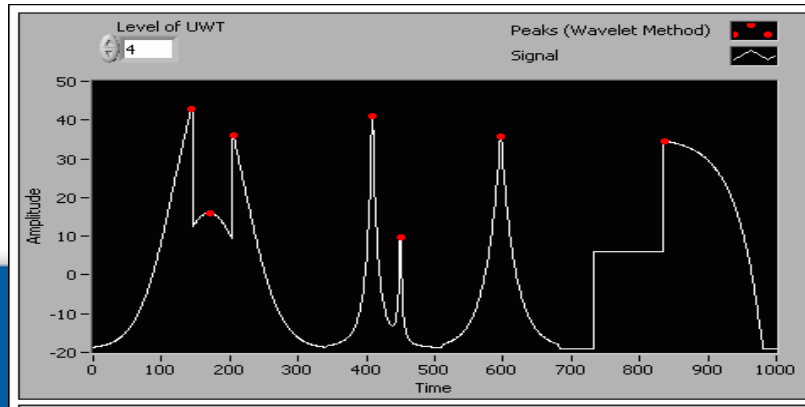


Digital filtering

Windowing



Resampling



LabVIEW FPGA IPNet

ni.com/ipnet

- Math
- Signal Processing
- Data Manipulation and Transfer
- RF and Communications
- Digital Protocols
- Data Acquisition
- Signal Generation
- Control
- Sensor Simulation

More than 200 IP cores and examples

HDL-Based IP in LabVIEW FPGA

- HDL Interface Node
  - Inline HDL integration
- Component-Level IP Node
  - Parallel HDL integration

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

Library XilinxCoreLib;
ENTITY filt IS
        port (
        ND: IN std_logic;
        RDY: OUT std_logic;
        CLK: IN std_logic;
        RST: IN std_logic;
        RFD: OUT std_logic;
        DIN: IN std_logic_VECTOR(15 downto 0);
        DOUT: OUT std_logic_VECTOR(30 downto 0));
END filt;

ARCHITECTURE filt_a OF filt IS

component wrapped_filt
        port (
        ND: IN std_logic
        RDY: OUT std_log
        CLK: IN std_logi
        RST: IN std_logi
        RFD: OUT std_log
        DIN: IN std_logi
        DOUT: OUT std_lo
end component;

-- Configuration specifi
        for all : wrappe
        generic map(

BEGIN

U0 : wrapped_filt
                port map

END filt_a;
```

```
Library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;


entity DemoClipAdder is
    port (
          clk : in std_logic;
          aReset : in std_logic;
          cPortA : in std_logic_vector(15 downto 0);
          cPortB : in std_logic_vector(15 downto 0);
          cAddOut : out std_logic_vector(15 downto 0) := (others => '0')
        );
end DemoClipAdder;


architecture rtl of DemoClipAdder is
begin
    process(aReset, clk) begin
      if(aReset = '1') then
        cAddOut <= (others => '0')
      elsif rising_edge(clk) then
        cAddOut <= std_logic_vector(signed(cPortA) + signed(cPortB));
      end if;
    end process;
end rtl;
```

Questions?

How to Learn More

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2 Day LabVIEW FPGA Module Course