Agenda

- Programming FPGAs
- Why Are They Useful?
- NI FPGA Hardware
- Common Applications for FPGAs
- How to Learn More
FPGA Technology

Logic Blocks

Programmable Interconnects

I/O Blocks
FPGA Logic Implementation

Implementing Logic on FPGA: $F = \{(A+B)CD\} \oplus E$

LabVIEW FPGA Code
Demo

• Filter
LabVIEW FPGA Code Abstraction

Counter

Analog I/O

I/O with DMA

Butterworth Filter

Write

Element

Timeout

Timed Out?

VHDL ~4000 lines

labview.com
LabVIEW FPGA Module

- LabVIEW code is translated to hardware circuitry implemented on the FPGA
- Natural representation of FPGA logic
Demo

• Simple I/O
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Why Are They Useful?

- **True Parallelism** – Provides parallel tasks and pipelining

- **High Reliability** – Designs become a custom circuit

- **High Determinism** – Runs algorithms at deterministic rates down to 25 ns (faster in many cases)

- **Reconfigurable** – Create new and alter existing task-specific personalities
True Parallelism
High Reliability and Determinism

Decision Making in **Software** Multiple **Software Layers**

- **UUT**
  - ~25 μs Response
  - Outputs

- Hardware
- Operating System
- Driver API
- Application Software

Calculation

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High Reliability and Determinism

Decision Making in Hardware

Highest Determinism

UUT

25 ns* Response

Outputs

Higher Reliability

Operating System

Driver API

Application Software

* Faster response for 80 and 120 MHz clocks
Demo

• AI, AO, Custom Threshold logic
From LabVIEW to Hardware

Translation → Optimization → Synthesis → Bit Stream

VHDL Generation → Analysis Logic Reduction → Place and Route Timing Verification → Generation Download/Run

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What Is RIO Technology?

• Use NI LabVIEW to design custom hardware circuitry with off-the-shelf devices
NI LabVIEW FPGA Hardware Targets

- **R Series Multifunction RIO**
  - General Purpose I/O for Measurement and Control

- **NI CompactRIO**
  - Industrial Control and Monitoring

- **NI SingleboardRIO**
  - Embedded Systems

- **NI FlexRIO**
  - Manufacturing Test and Design Validation

- **Other**
  - RIO IF Transceiver
  - PCIe Framegrabbers
  - Compact Vision System

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Common Applications

- High-speed control
- Custom DAQ
- Digital communication protocols
- Sensor simulation
- Onboard processing and data reduction
Common Applications

• High-speed control
• Custom DAQ
• Digital communication protocols
• Sensor simulation
• Onboard processing and data reduction
• Coprocessing
High-Speed Control

About 200 kHz loop rate
Common Applications

- High-speed control
- Custom DAQ
- Digital communication protocols
- Sensor simulation
- Onboard processing and data reduction
Customize Your DAQ Device

• Custom timing & synchronization
• Multi-rate sampling
• Custom triggering
• Custom counters
• Flexible PWM
• Flexible encoder interface
Custom Triggered Analog Input
Common Applications

- High-speed control
- Custom DAQ
- Digital communication protocols
- Sensor simulation
- Onboard processing and data reduction
Digital Communication

Example – SPI

CS

SCLK

MOSI

Entire Sample Time 275 ms

Begin Transfer by pulling CS_bar Low

Data Delay

SCK High

SCK High

Falling Edge

End Transfer by pulling CS_bar High

Temperature Bits

SPI Temperature Transfer Loop
Common Applications

- High-speed control
- Custom DAQ
- Digital communication protocols
- Sensor simulation
- Onboard processing and data reduction
Sensor Simulation and FPGA

- Fully customizable hardware – Many types of sensors
- Parallelism – Many sensors on chip with no interference
- Strict timing requirements – Deterministic or highly realistic
- Onboard processing – Engineering units to sensor signals
Common Applications

- High-speed control
- Custom DAQ
- Digital communication protocols
- Sensor simulation
- Onboard processing and data reduction
Onboard Processing and Data Reduction

Built-In I/O
- Analog voltages
- Digital communications
- Sensor signals

Input

Processing
- Encoding/decoding
- Filtering/averaging
- Modulation/demodulation
- Decimation
- Stream processing

Process

Output
- DMA preprocessed data
- Streaming from input to output without host involvement

Output

DMA to Host

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NATIONAL INSTRUMENTS
Intellectual Property (IP)

FFT
DC/RMS
Waveform Averaging
Digital filtering
Windowing
Resampling

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HDL-Based IP in LabVIEW FPGA

• HDL Interface Node
  ▪ Inline HDL integration

• Component-Level IP Node
  ▪ Parallel HDL integration
How to Learn More

ni.com/fpga

Questions?

ni.com/training

2 Day LabVIEW FPGA Module Course